

FIG. 2

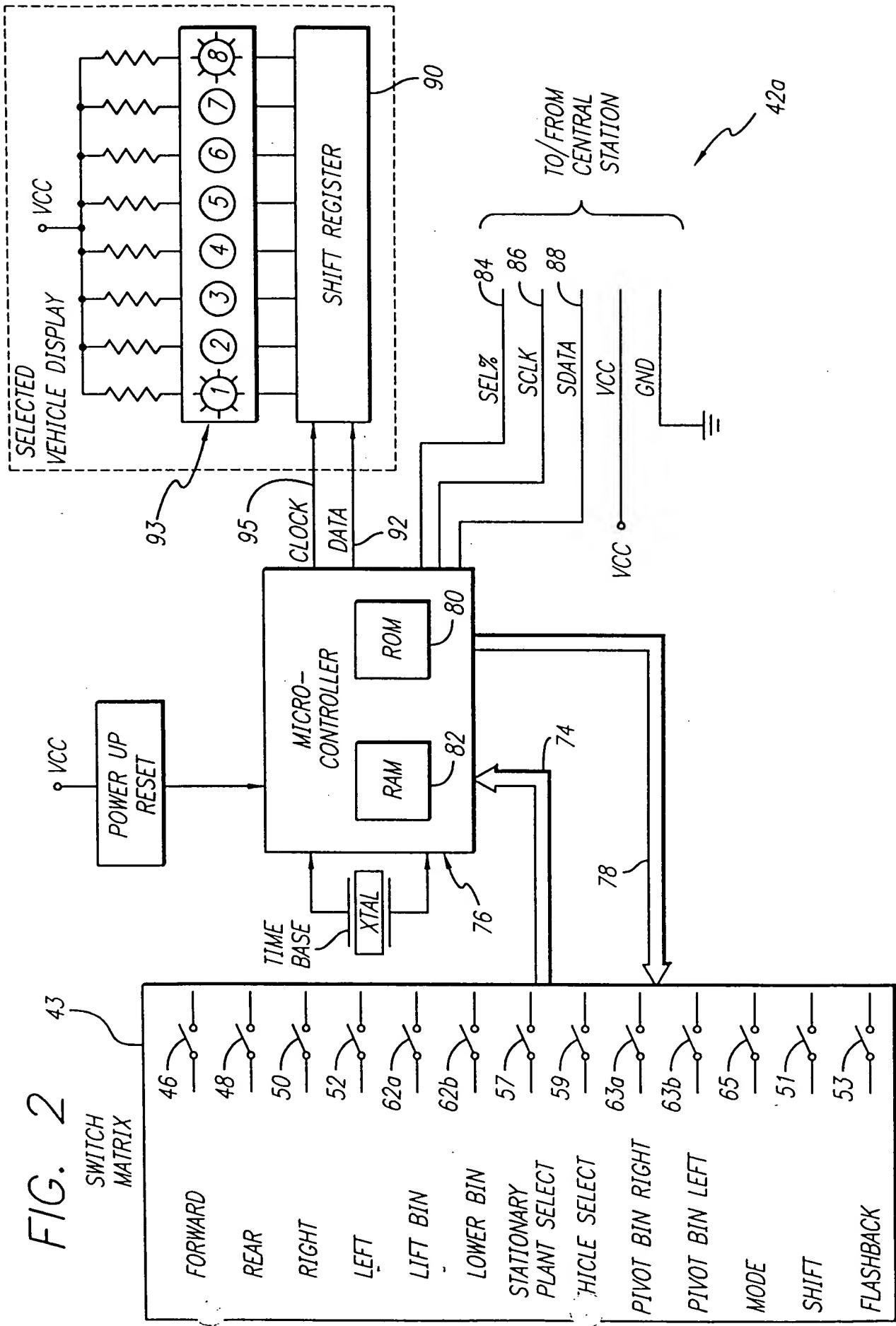
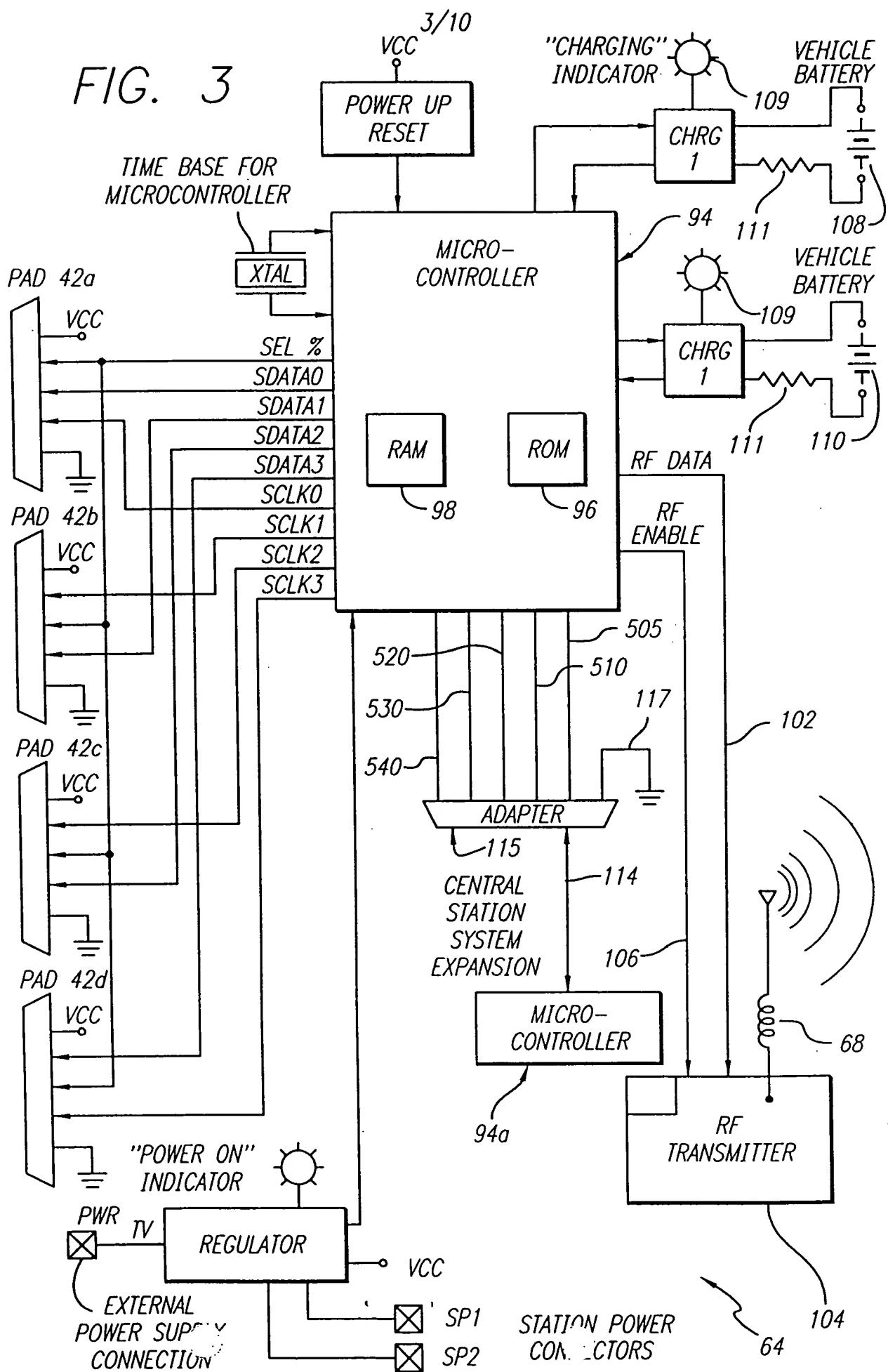


FIG. 3



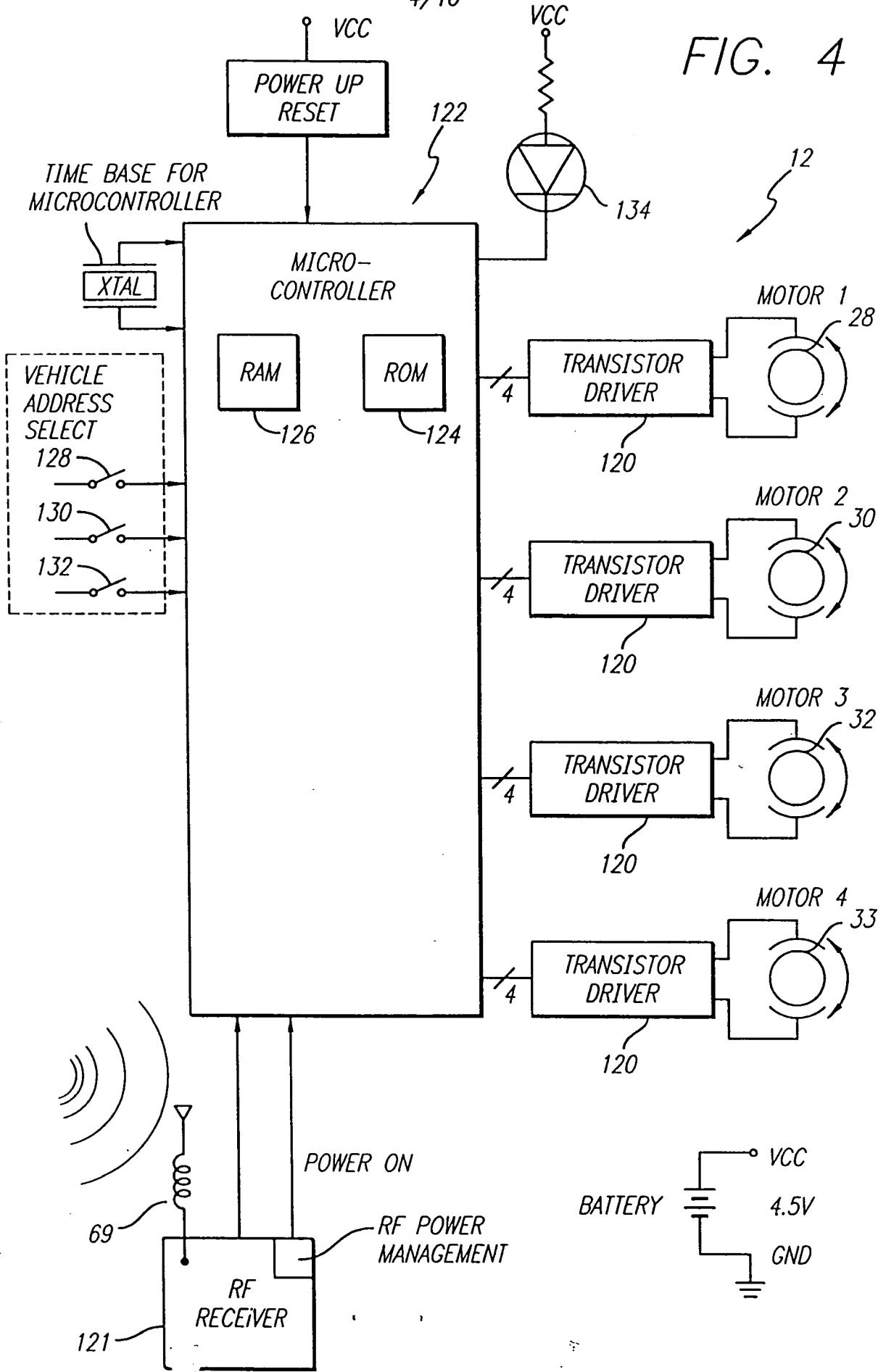


FIG. 5

FIG. 6A

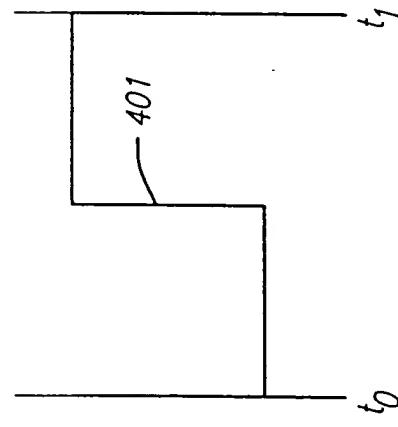


FIG. 6B

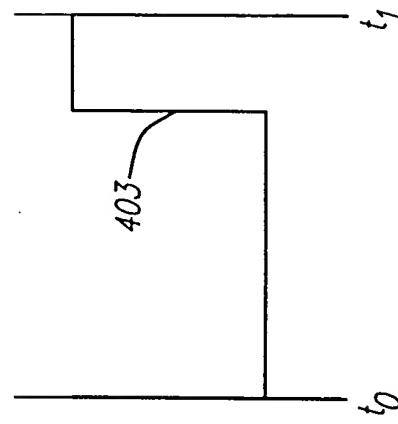
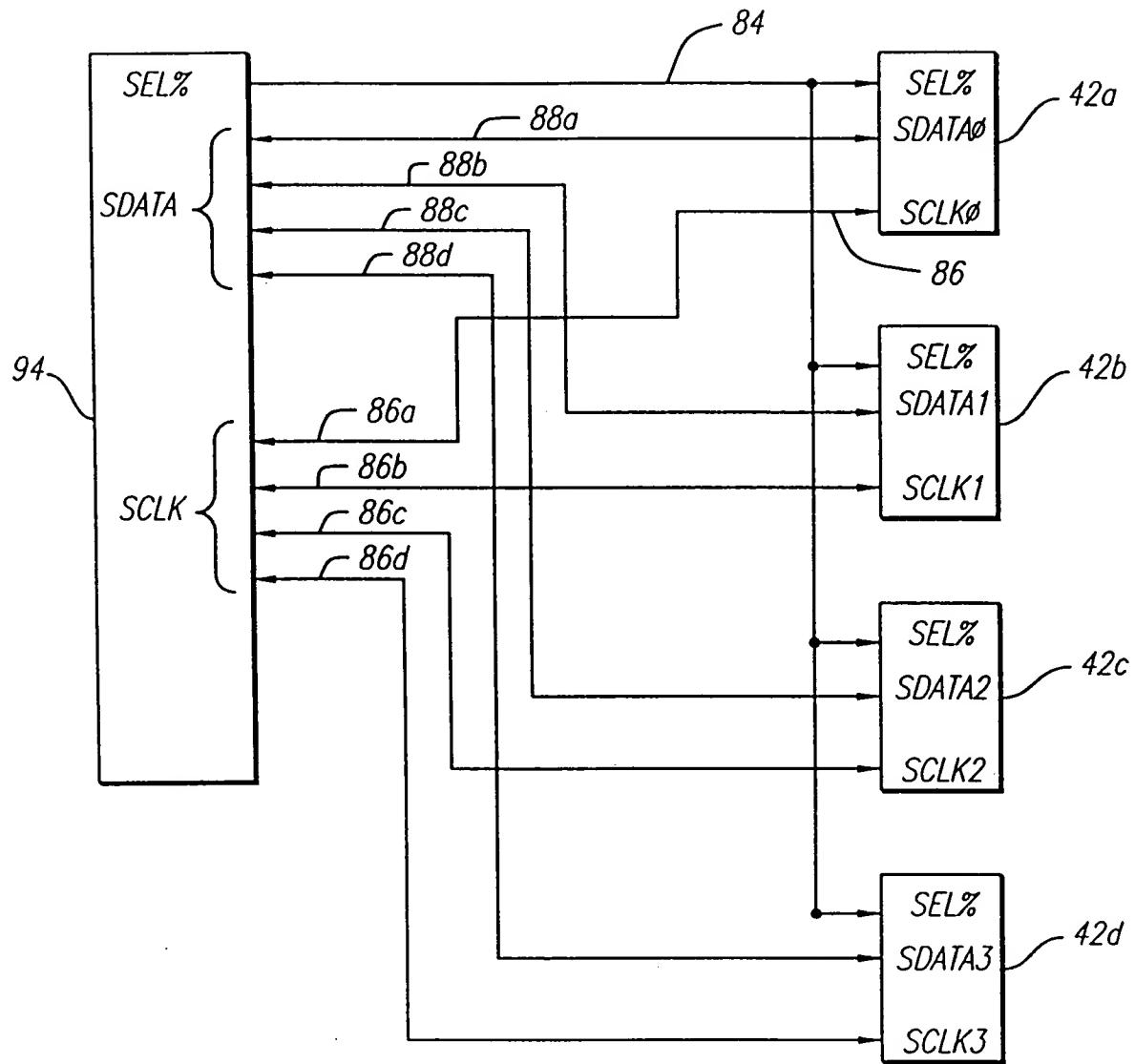


FIG. 7



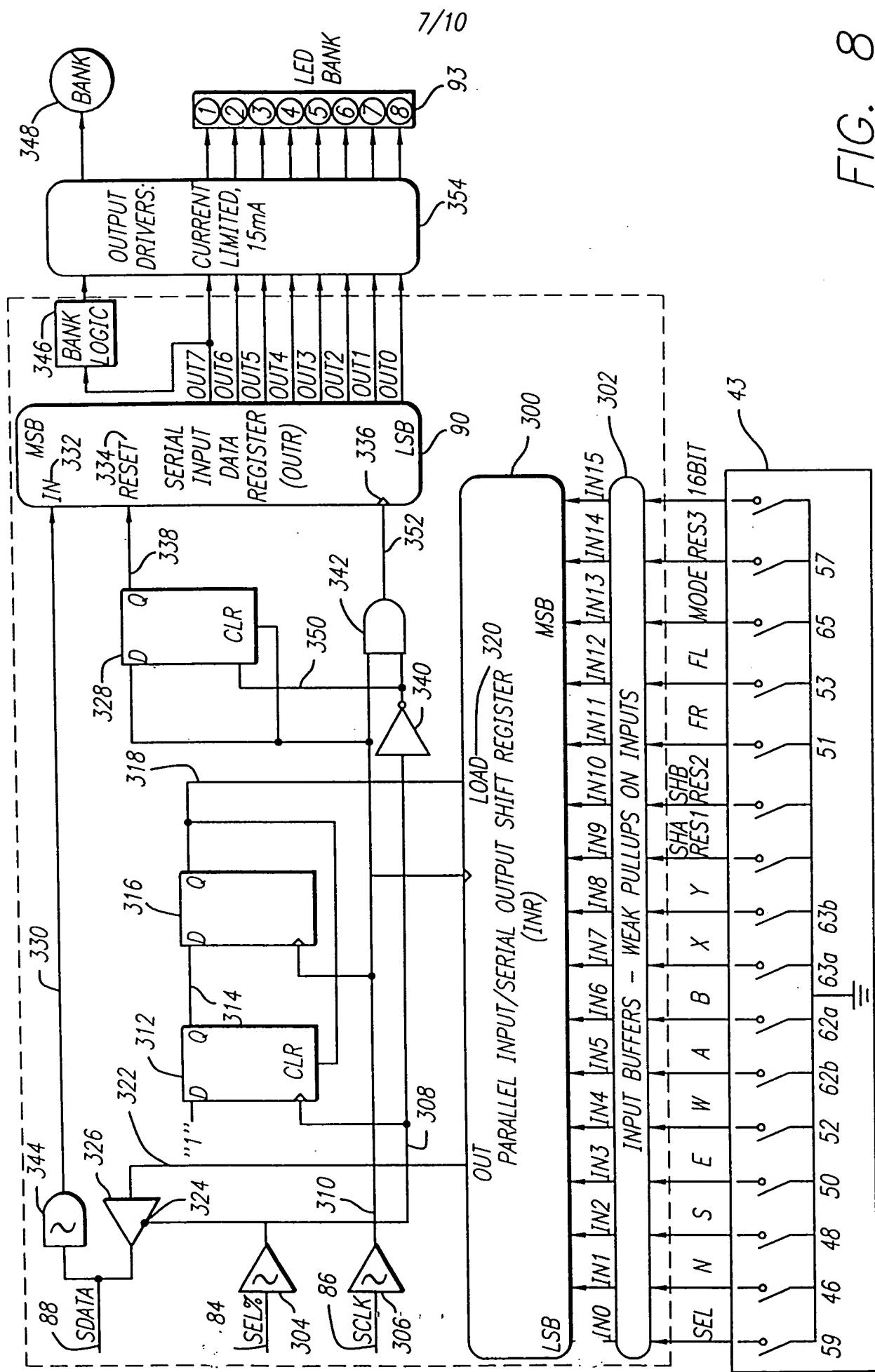
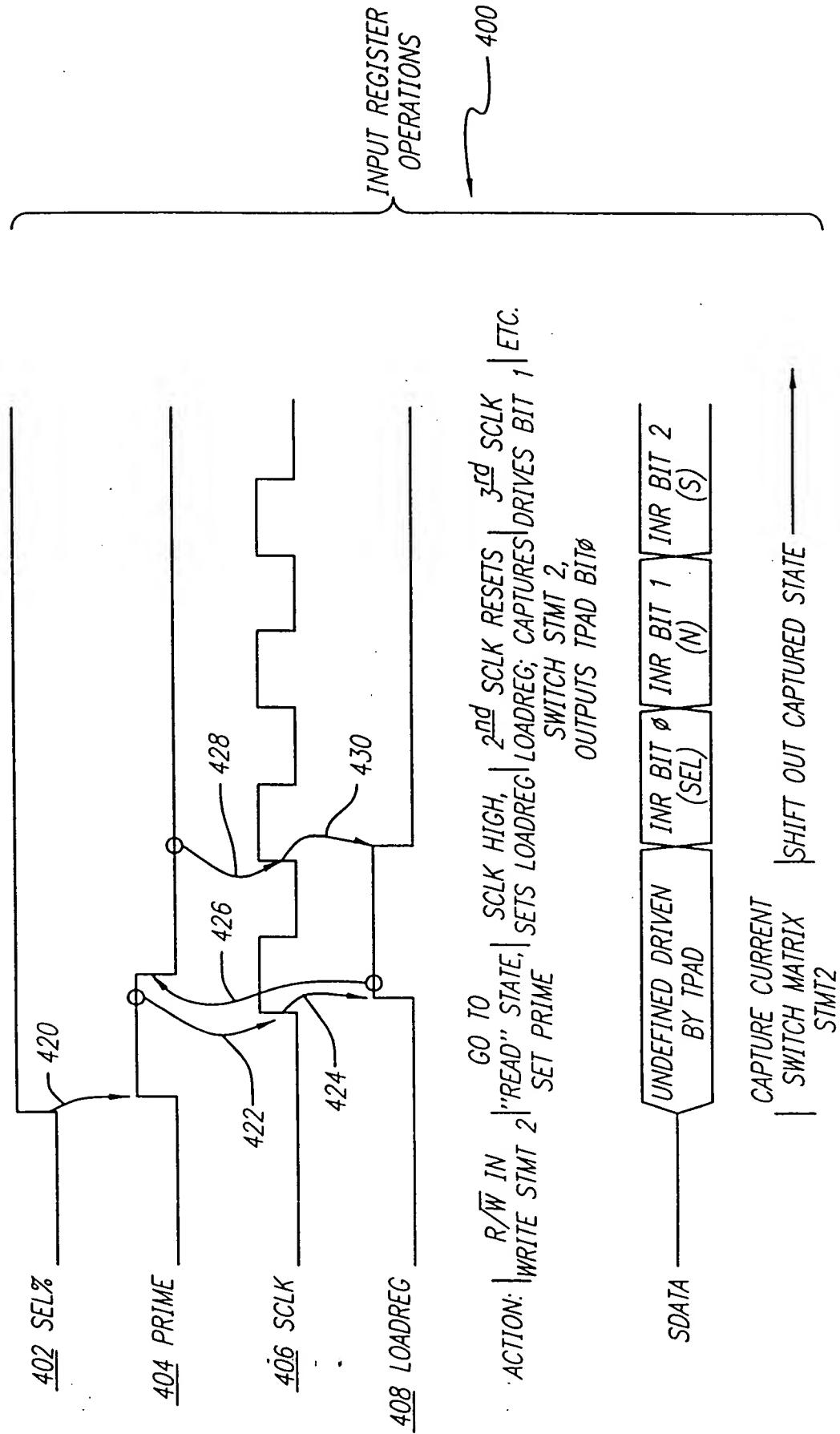


FIG. 8

FIG. 9-1



ACTION: | R/W IN | GO TO | SCLK HIGH, | 2nd SCLK RESETS | 3rd SCLK | ETC.  
 | WRITE STMT 2 | "READ" STATE, | SETS LOADREG | CAPTURES | DRIVES BIT 1 |  
 | SET PRIME | SETS LOADREG | LOADREG; SWITCH STMT 2;  
 | OUTPUTS | TPAD BIT@

FIG. 9-2

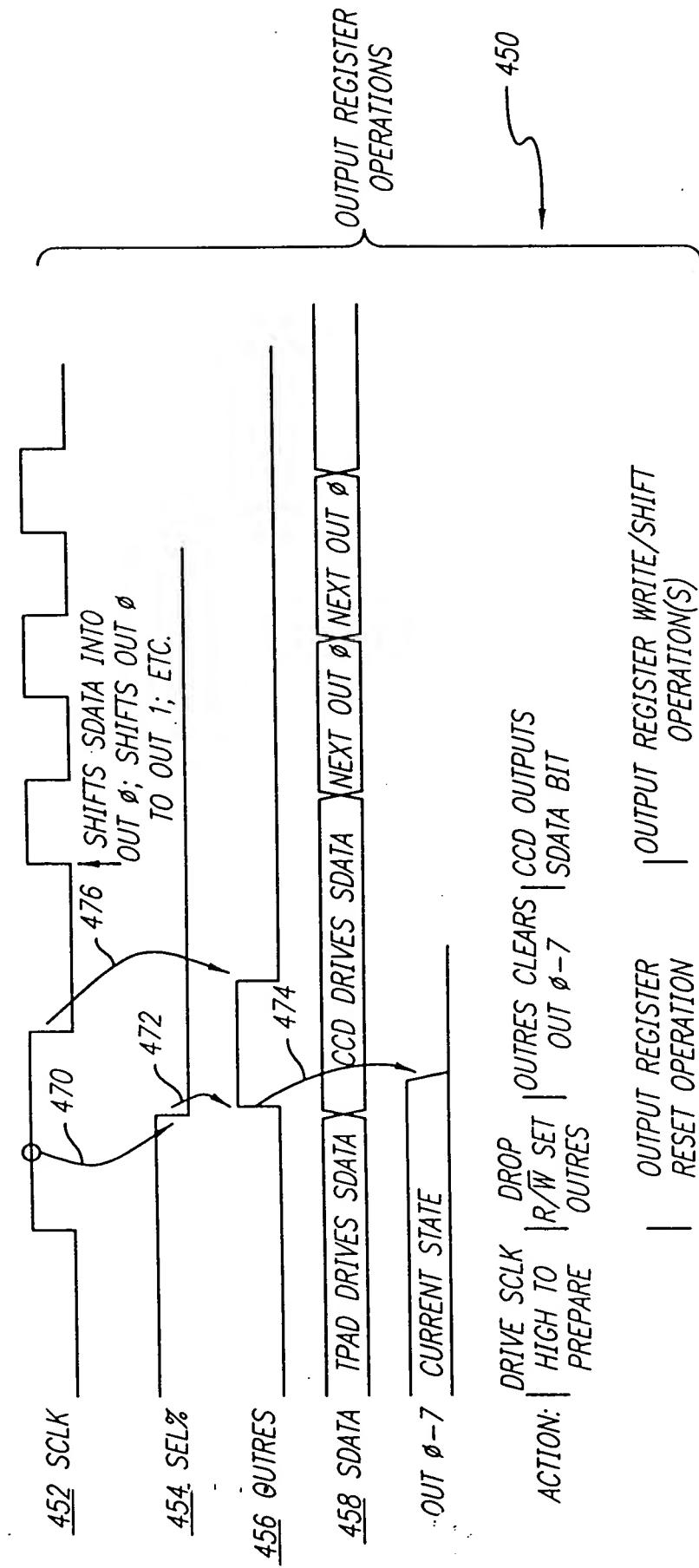
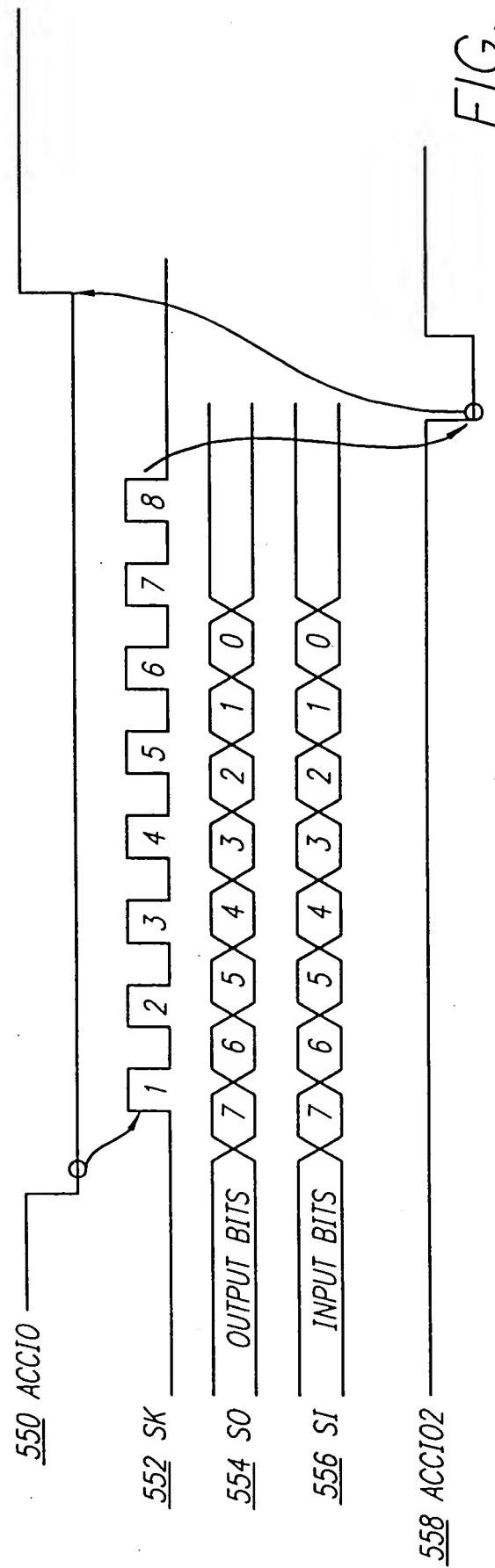
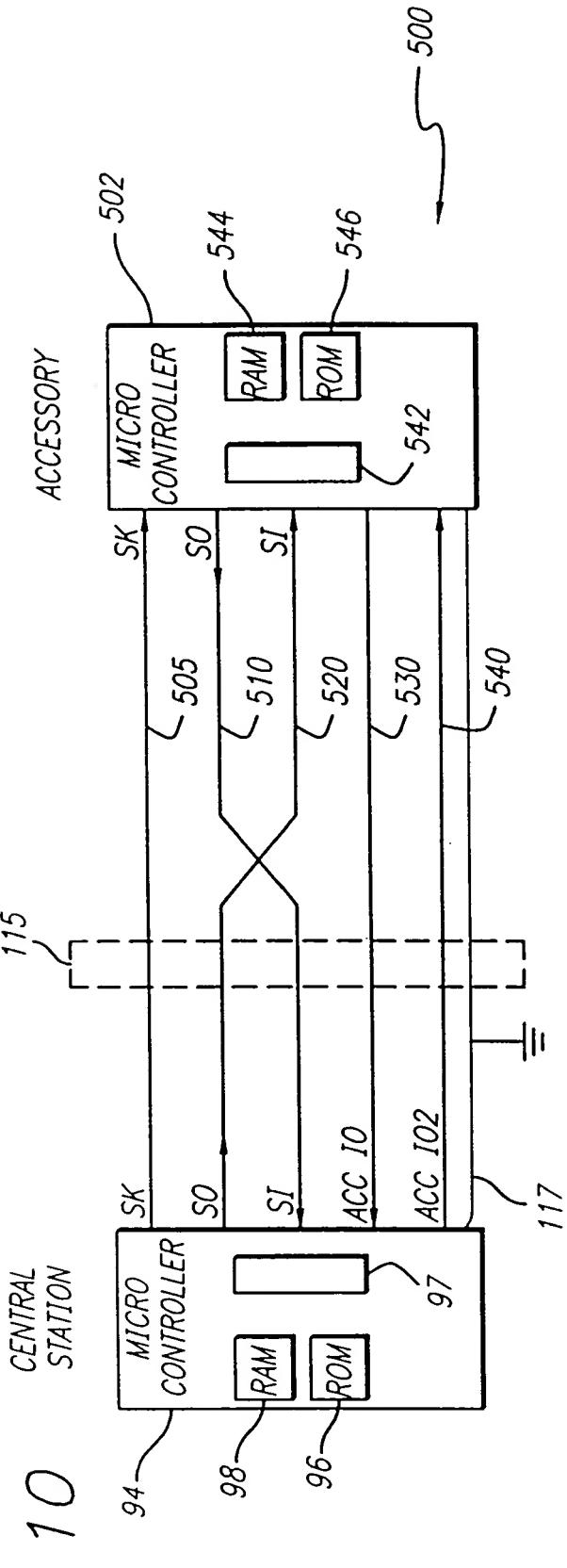
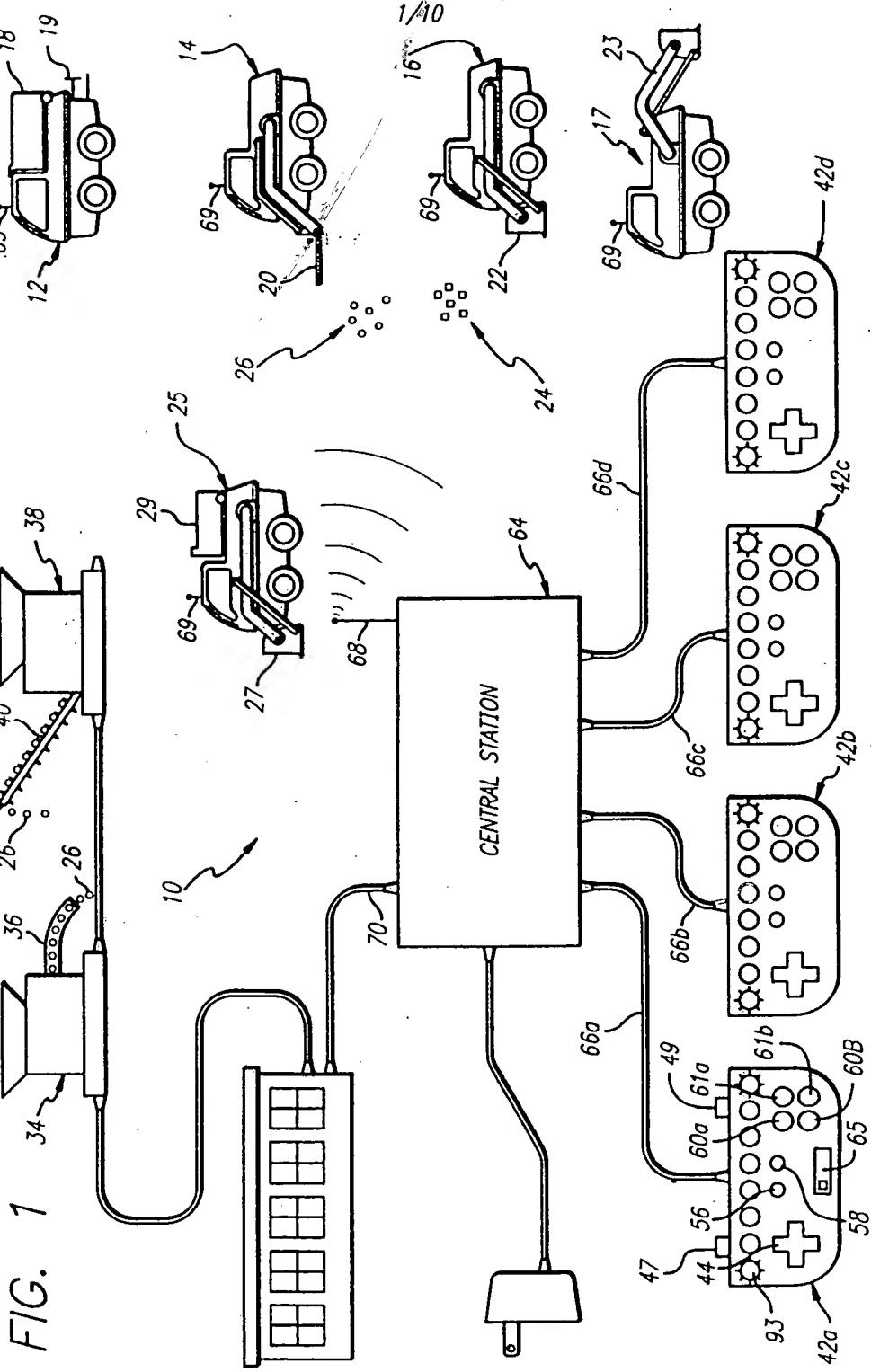


FIG. 10





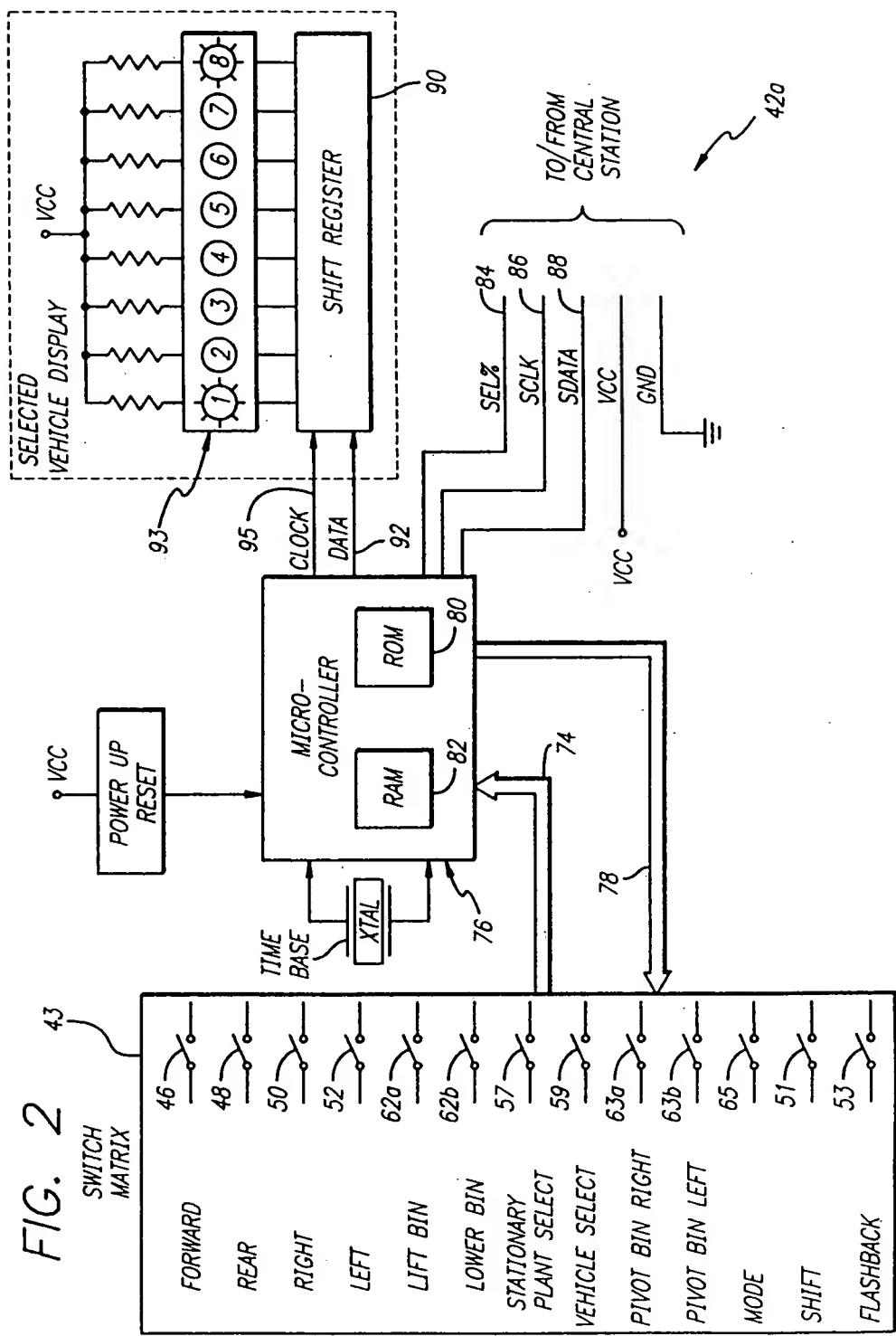
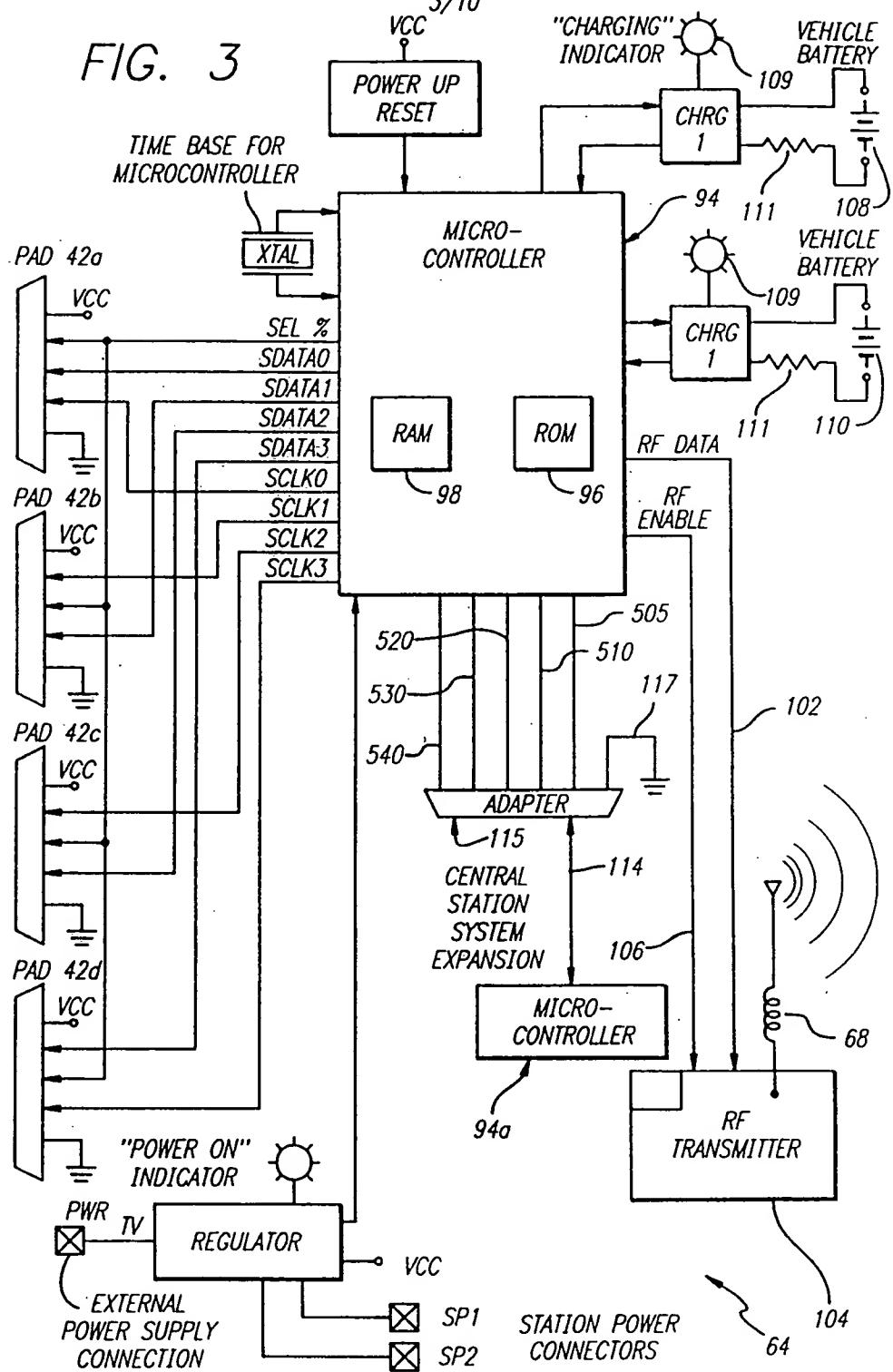
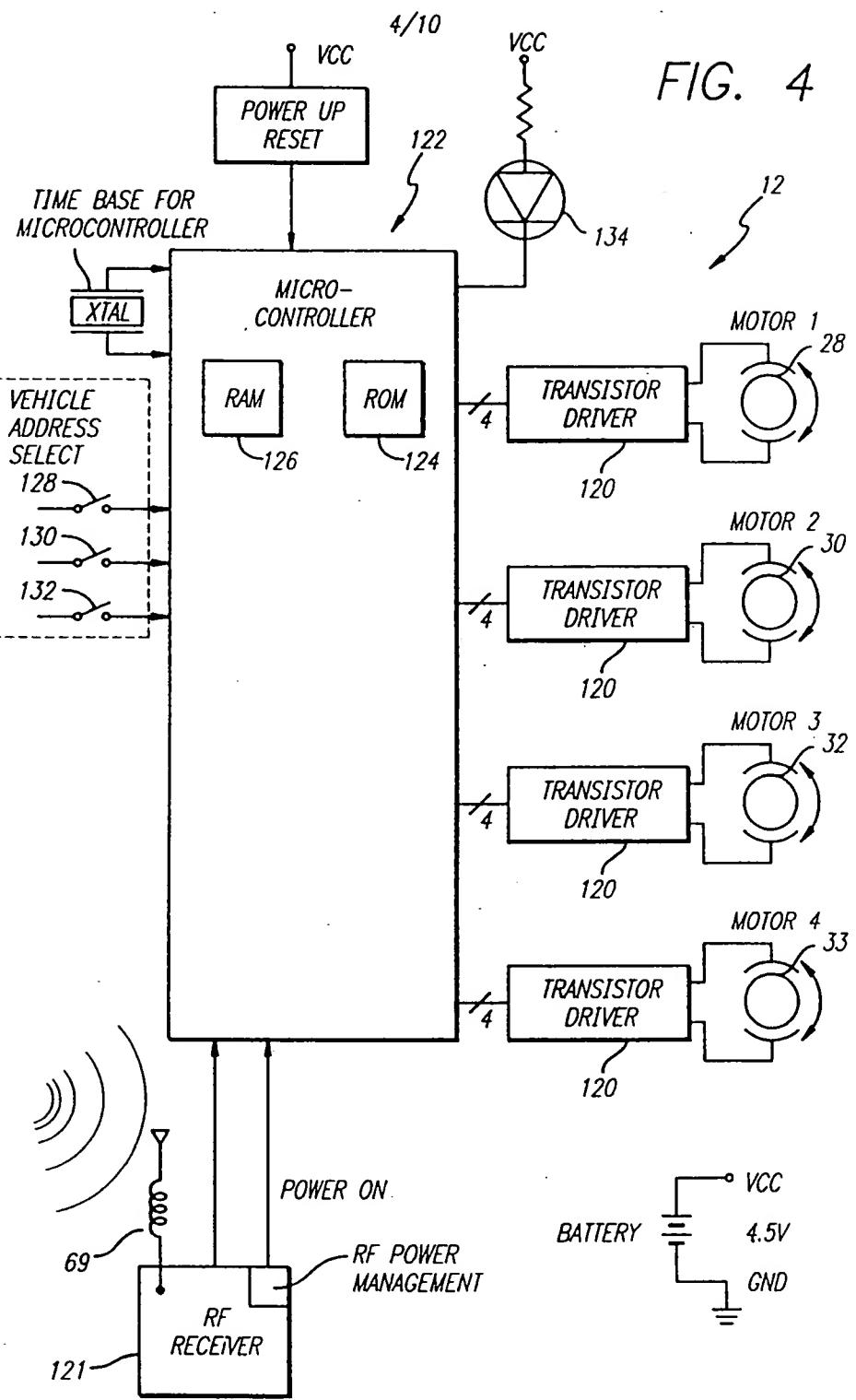


FIG. 3

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BEST AVAILABLE COPY

FIG. 5

FIG. 6A

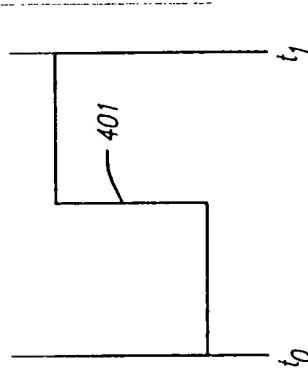


FIG. 6B

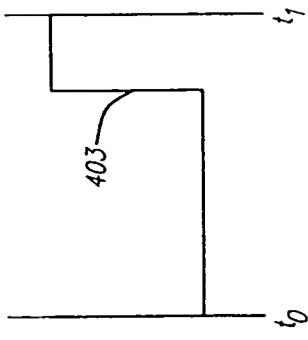


FIG. 7

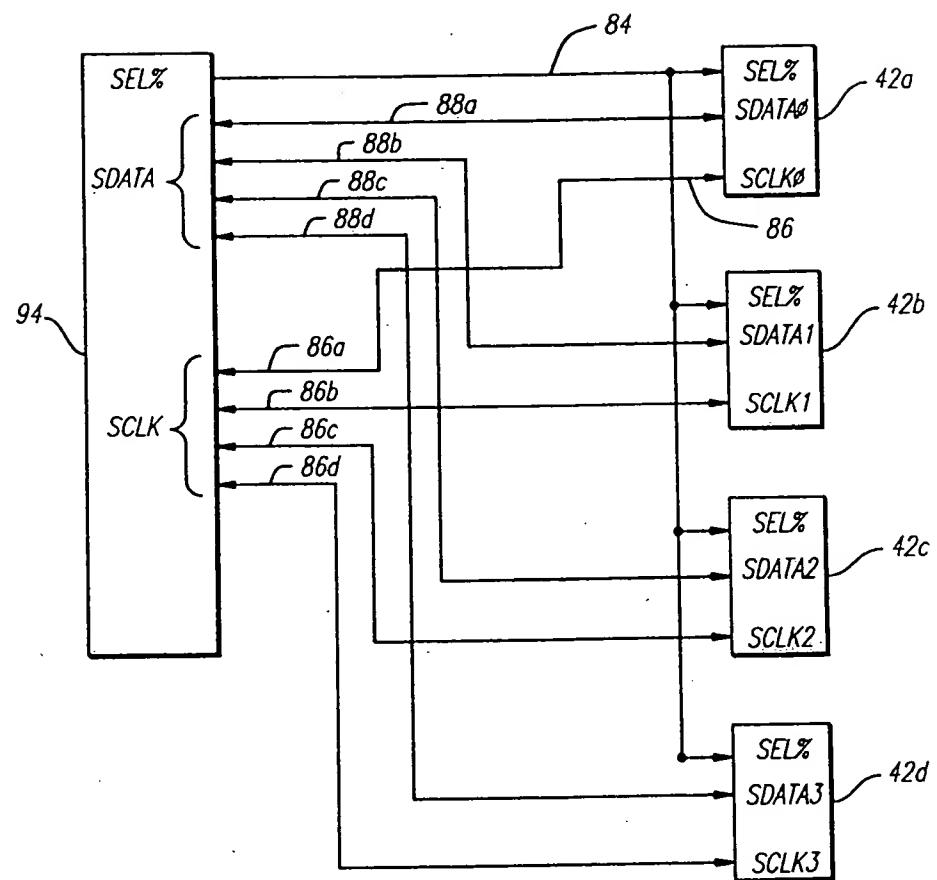


FIG. 8

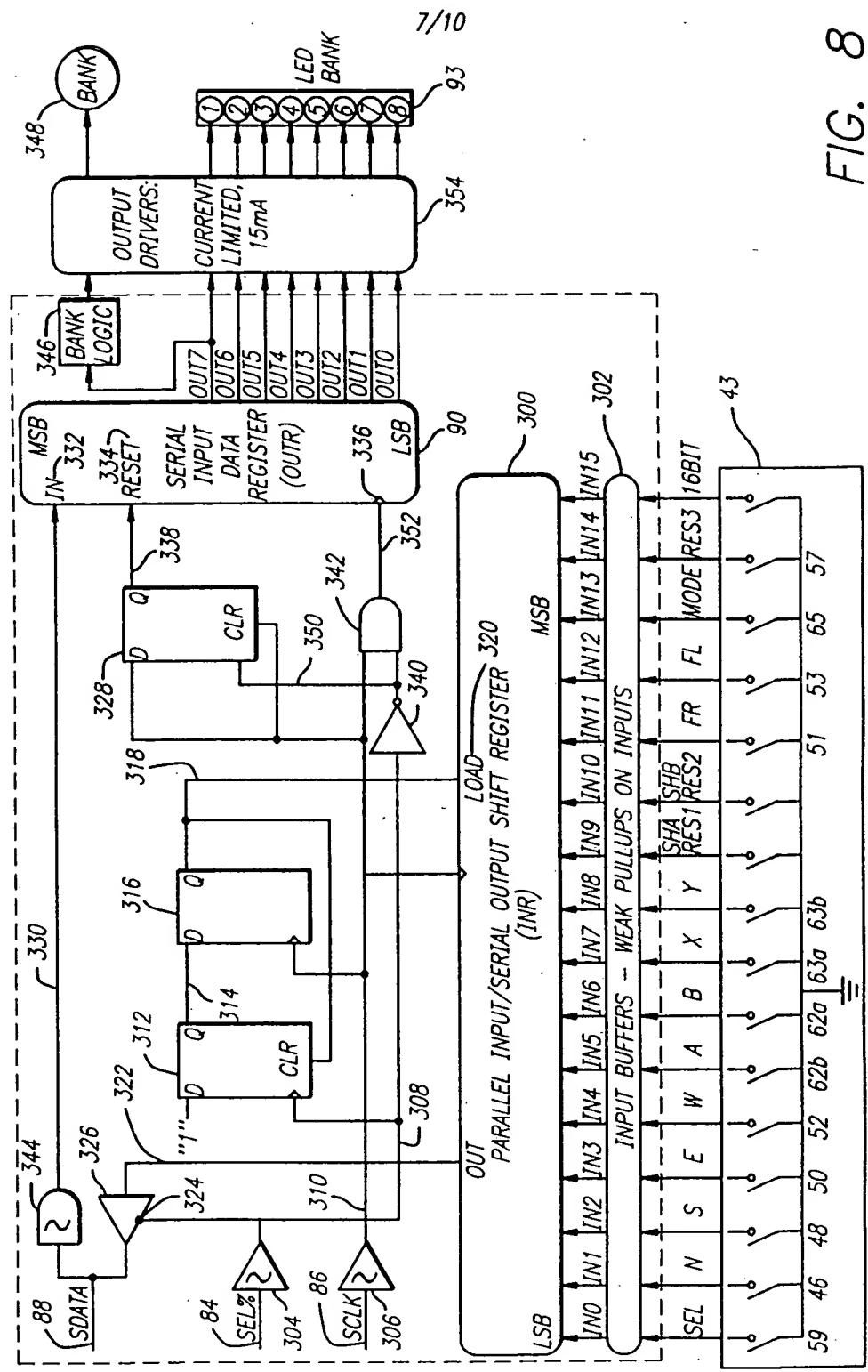


FIG. 9-1

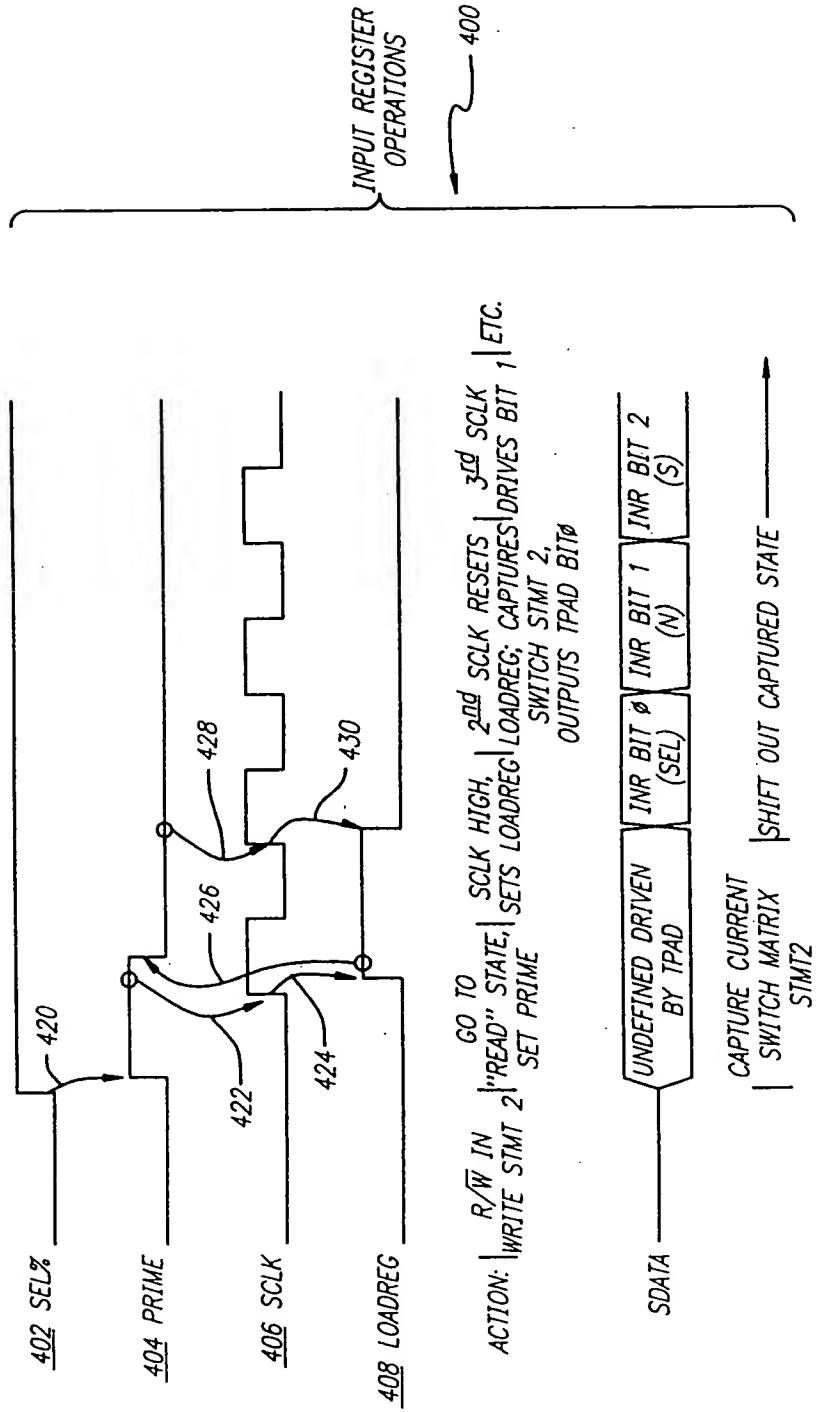


FIG. 9-2

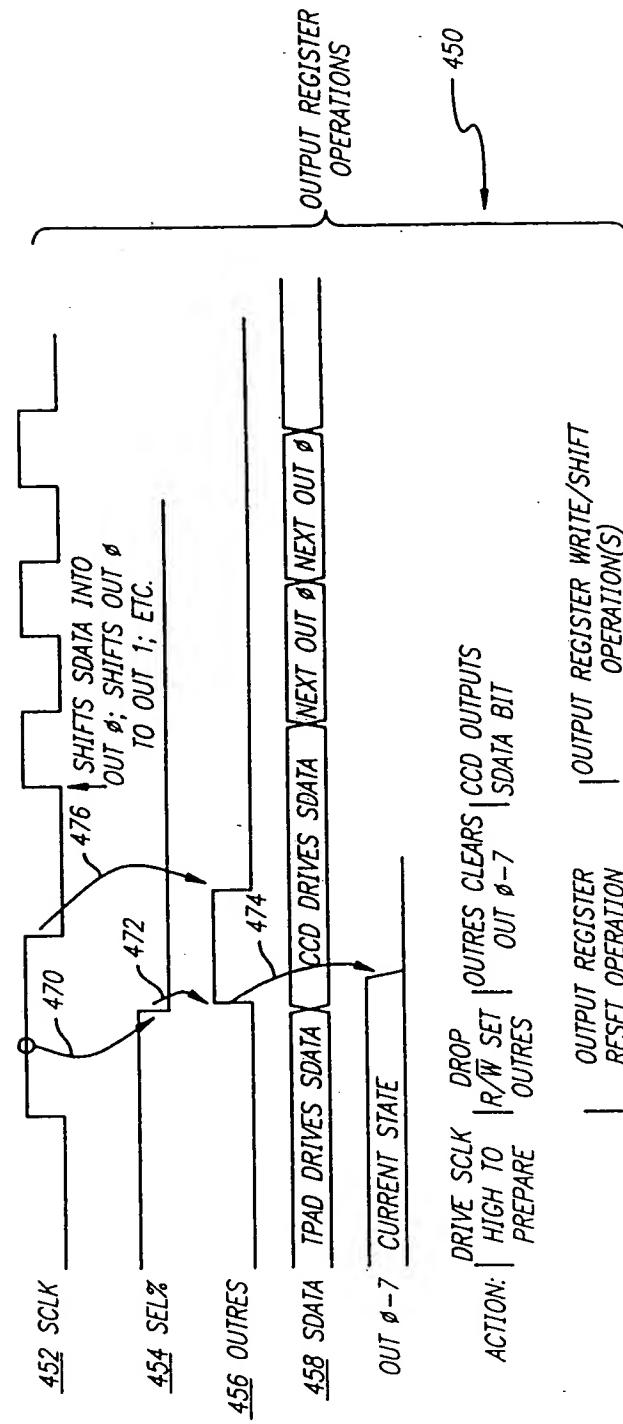
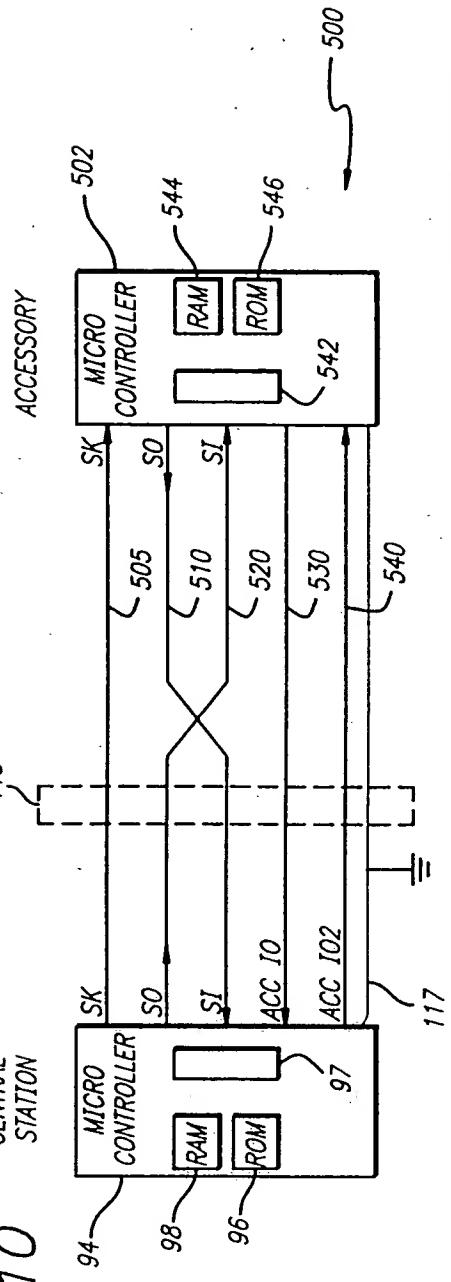


FIG. 10

CENTRAL  
STATION

115



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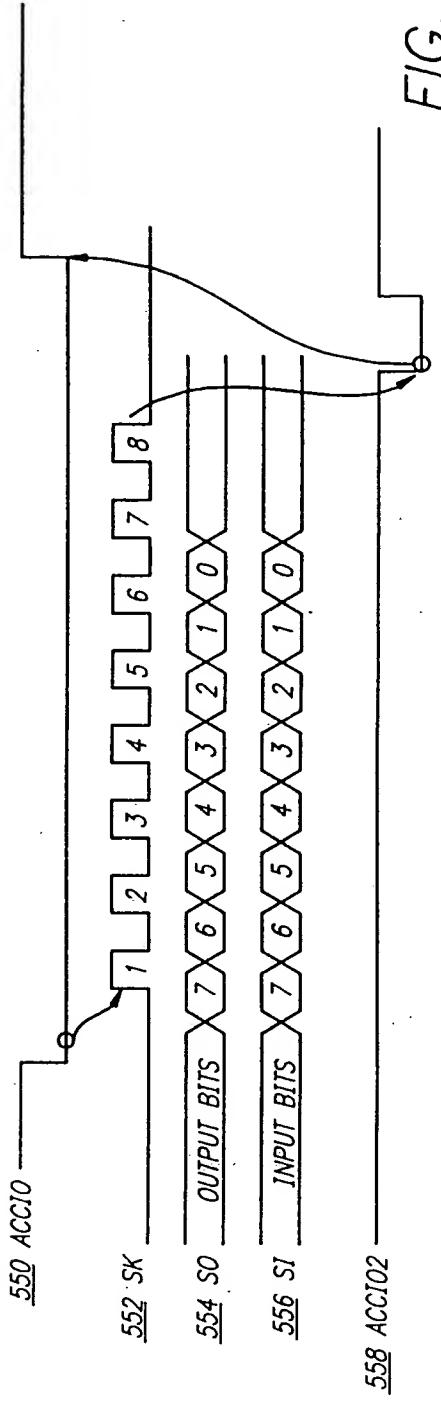


FIG. 11